International Journal of Innovative Research in Electronics and Communications (IJIREC)
*Volume 6, Issue 4, 2019, PP 18-24*
*ISSN 2349-4050 (Online) & ISSN 2349-4042 (Print)*
*DOI: http://dx.doi.org/10.20431/2349-4050.0604002*
*www.arcjournals.org*

# Research of Nanoscale MOSFET Parameters Impact on the Performance of Energy Converters for Internet of Things

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**Abstract:** *Wireless microdevices are widely adopted in Radio-frequency Identification (RFID), Wireless Sensor Networks (WSN), Internet of Things (IoT). Among them, passive devices have a special place, since they haven't constant internal power supply. Passive devices are cheaper and more compact than their active analogs, their lifetime is higher, and they can be applied in some applications, which are inappropriate for active tags, e.g. in medical implants. However passive devices have to receive the energy for operation from the outside through RF radiation - from reader or harvesting energy from the environment. For conversion this energy to power supply voltage of passive microdevice IC, voltage rectifiers are used. The purpose of this work is research of impact on output voltage by parameters of nanoscale diode-connected MOSFETs, which perform functions of rectifiers in the energy converters. The comparison of different voltage rectifier configurations was made based on Tanner EDA simulation results. The current-voltage characteristics of diode-connected MOSFETs were obtained for different CMOS technologies. The impact of transistor threshold voltage and its sizes on output voltage of single-stage multiplier for different technologies, input voltage amplitudes and load resistances was investigated. The results of the research can be useful in the design of wireless passive microdevices.*

**Keywords:** *Internet of Things, RFID, energy converters, nanoscale MOSFETs, subthreshold design, transient simulation..*

## 1. INTRODUCTION

Nowadays the devices with wireless supply are increasingly used in industry, commerce, logistics, construction as well as in everyday life. So Internet of Things technologies allow forming 'intellectual' nets of physical objects, interacting between each other through RF radiation, thanks to which the creation of diverse automated systems like smart home is possible [1-6]. By means of Wireless Sensor Networks [1, 2, 4, 6-9] one can in real-time mode monitor the state of various complex systems and objects, e.g. durability degree of a building or a bridge. In Radio-frequency Identification technology [4, 6-16] miniature devices called tags or transponders are deployed. The tags are attached to different objects in production facilities, shopping centers and warehouses for implementation the automated identification and also used in access control systems. Thus in all of the above applications wireless micro devices are used. These micro devices exchanges data with the base station interacting with computer system resulting in automated identification, surveillance and management are carried out.

Compact wireless devices (radiofrequency tags, sensors and others) are divided into active and passive ones. Active tags [8, 16] are equipped by embedded power supply (battery) and passive ones [7-9, 12, 13] obtain energy for the operation through RF radiation from related to them base station (reader) or harvest energy from the environment [1-4, 6, 7, 9-11, 15]. Due to battery supplying, operating range of the active tags is higher than range of passive ones. However the active tags are significantly second to the passive tags in cost, weight and sizes. Moreover in some applications, e.g. in medical implants, applying of the passive tags is preferable since their lifetime is higher than the active analogues, in which it is limited by battery life.

Due to the passive tags obtain the energy for operation from outside, their input voltage amplitude reduces with increasing the distance between the tag and the reader resulting in the operation range of such devices is usually limited by some meters. However there are fields (e.g. large warehouses or production rooms) where low self-cost and small sizes, i.e. the advantages of passive microdevices, and at the same time the possibility of functioning at a considerable distance from base station are required. Furthermore in the case when the passive devices harvest energy for supplying from the outside (from radio- and TV-stations, cellular communication stations, Wi-Fi and Bluetooth devices) the input voltage amplitude can be low too. That’s why the research and development of passive devices which able to work at very low input voltages is relevant challenge.

Currently for conversion the radiofrequency energy incoming to the passive microdevices to power supply voltage, the rectifiers based on nanoscale diode-connected MOSFETs [1, 3, 7, 9, 11-14] or Schottky diodes [1, 2, 4, 6, 9, 10, 15] are applied. Because of Schottky diodes’ low voltage drop at direct connection and high switching rate, the output voltage and conversion rate of rectifiers based on them are higher than in the case of rectifiers based on MOS transistors. However the manufacture of rectifiers based on Schottky diodes is more expensive since they are not compatible with conventional CMOS technologies.

## 2. RESEARCH OF ENERGY CONVERTERS

There are several configurations of the voltage rectifiers using in the passive tags. Figure 1,a shows the single-stage multiplier (doubler) circuit based on diode-connected nMOS transistors [1, 14]. In the case of ideal diodes and absence of capacitive losses, such circuit should double the value of input voltage but it does not occur in practice [17]. The circuit of the differential-drive bridge rectifier based on MOSFETs [9, 14] is shown in Figure 1,b. The circuit of the differential-drive gate cross-connected bridge rectifier [7, 9, 14] (Figure 1,c) was suggested for lowering power consumption determined by leakage currents and also for decreasing forward voltage drop compared to conventional bridge rectifier.

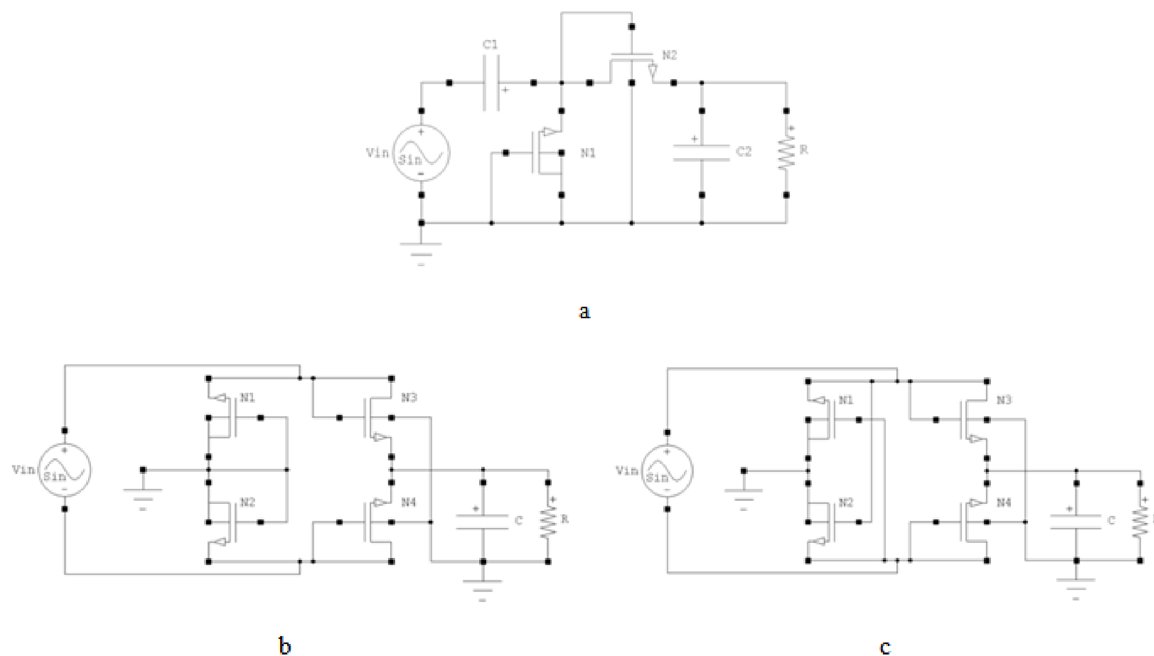


**Figure1.** *Circuit diagrams of different voltage rectifier configurations based on nMOS transistors: a) single-stage voltage multiplier; b) bridge rectifier; c) gate cross-connected bridge rectifier*

For comparison different rectifier configurations based on MOS transistors by output voltage level, the investigation of the transients taking place in described circuits during voltage rectification was conducted using Tanner EDA circuit simulation environment (T-Spice) [18]. BSIM4v4.8 model [19] considering physical features of nanoscale MOS transistors was used. Model parameters correspond to parameters of nMOS transistors with low leakage currents implemented by 90 nm CMOS

technology [20]. The capacitance of capacitors in use was 500 fF and frequency of input sinusoidal signal was 2.45 GHz. The comparison of different rectifier configurations simulation results is shown in Figure 2.

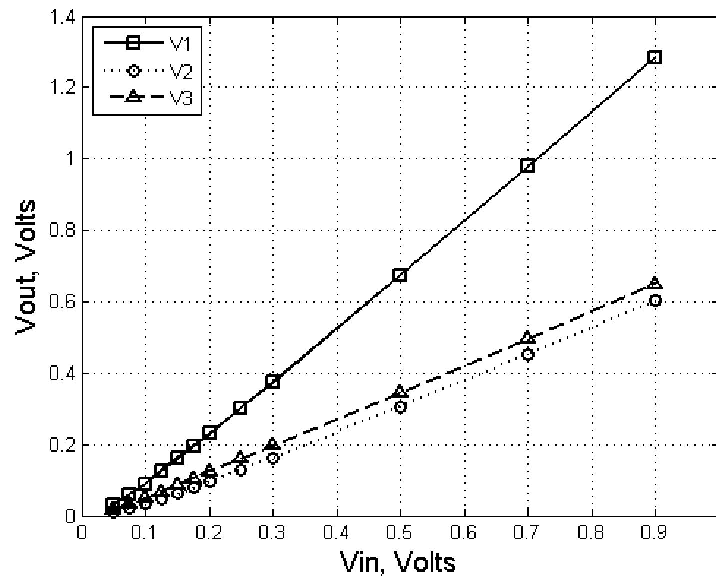


**Figure2.** O*utput voltage versus input voltage amplitude for different rectifier configurations: V1) single-stage voltage multiplier; V2) bridge rectifier; V3) gate cross-connected bridge rectifier*

It can be seen from Figure 2 that the highest values of rectified voltage through whole range of input voltages is reached under using the single-stage voltage multiplier. Higher output voltages could be obtained by increasing number of rectifier stages.

The choice of gate cross-connected bridge rectifier circuit allows to increase the output voltage by 55% in subthreshold region (for input voltages less than 0.28 V) and by 18% in strong inversion and saturation regions with respect to conventional bridge rectifier output voltage values.

## 3. Research of MOSFET Parameters Impact on the Output Voltage

The current flowing between drain and source in the diode-connected MOS transistor in the strong inversion region (over threshold voltage) is defined by expression [21]:

$$I_{ds,1} = \frac{1}{2} \mu \cdot \frac{\varepsilon \cdot \varepsilon_0}{d} \cdot \frac{W}{L} \cdot (V_d - V_{th})^2 \cdot (1 + \lambda \cdot V_d), \tag{1}$$

where μ - electron mobility, ε – SiO2 permittivity, ε0 – electric constant (vacuum permittivity), d – gate oxide thickness, W – transistor channel width, L – transistor channel length, Vd – diode-connected transistor voltage, Vth – threshold voltage, λ – channel length modulation parameter.

The subthreshold current of the diode-connected MOS transistor is defined by expression [21, 22]:

$$I_{ds,2} = \mu \cdot \frac{\varepsilon \cdot \varepsilon_0}{d} \cdot \frac{W}{L} \cdot (n-1) \cdot \varphi_T{}^2 \cdot exp\left(\frac{V_d - V_{th}}{n \cdot \varphi_T}\right) \cdot \left(1 - exp\left(\frac{-V_d}{\varphi_T}\right)\right), \tag{2}$$

Where n – slope parameter of current-versus-voltage transistor characteristic in subthreshold region (weak inversion region) [19], φT – thermal potential.

Figure 3 shows current-versus-voltage characteristics of nanoscale diode-connected MOSFETs implemented using different technologies. Characteristics were plotted using Tanner EDA program with model BSIM4 parameters from [20]. It can be seen from Figure 3 that the values of forward and reverse currents of diode-connected transistor in deep subthreshold region (Vd < 0.05 V) are comparable in order of magnitude, which reduces the diode rectifying ability and has a negative impact on charge-discharge processes of capacitors in voltage rectifiers.

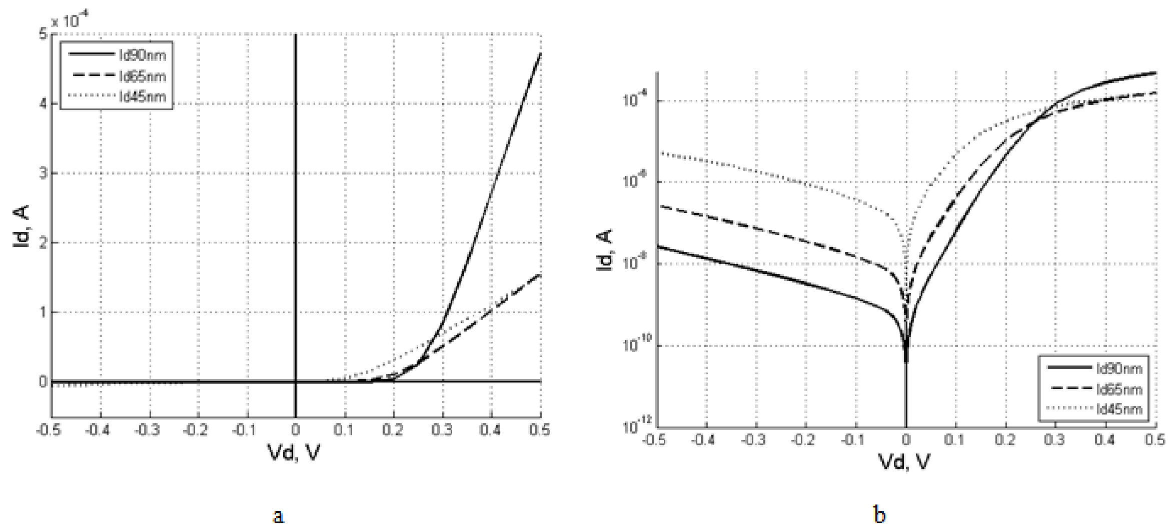


**Figure3.** *Current-versus-voltage characteristics of the diode-connected MOS transistors implemented using 90 nm, 65 nm and 45 nm technologies: a) linear scale; b) semi-logarithmic scale*

Among the parameters in expressions (1) and (2), the most interesting ones for design engineers are threshold voltage Vth and transistor sizes (relation W/L). The threshold voltage of nanoscale MOS devices can be written as [20]:

$$V_{th} = V_{THO} + K_1 \cdot \left(\sqrt{\Phi_s - V_{bs}} - \sqrt{\Phi_s}\right) - K_2 \cdot V_{bs} + \Delta V_{SCE} + \Delta Vt_{NULD} + \Delta V_{DIBL}, \quad (3)$$

where VTH0 – long-channel threshold voltage at Vbs = 0 V, Vbs – bulk-source potential, K1 and K2 – first- and the second-order body bias coefficient respectively, Φs – surface potential, ΔVSCE – the short channel effect on Vth, ΔVNULD – the non-uniform lateral doping effect on Vth, ΔVDIBL – the drain-induced barrier lowering effect (DIBL) on Vth [19, 22]. At technology development parameter VTH0 is determinant.

The degree of threshold voltage VTH0 impact on output voltage level Vout of the single-stage voltage multiplier (Figure 1,a) for 90 nm and 65 nm CMOS technologies with various values of load resistances R and input voltage amplitudes Vin was investigated using Tanner EDA. The simulation results are shown in Figure 4.

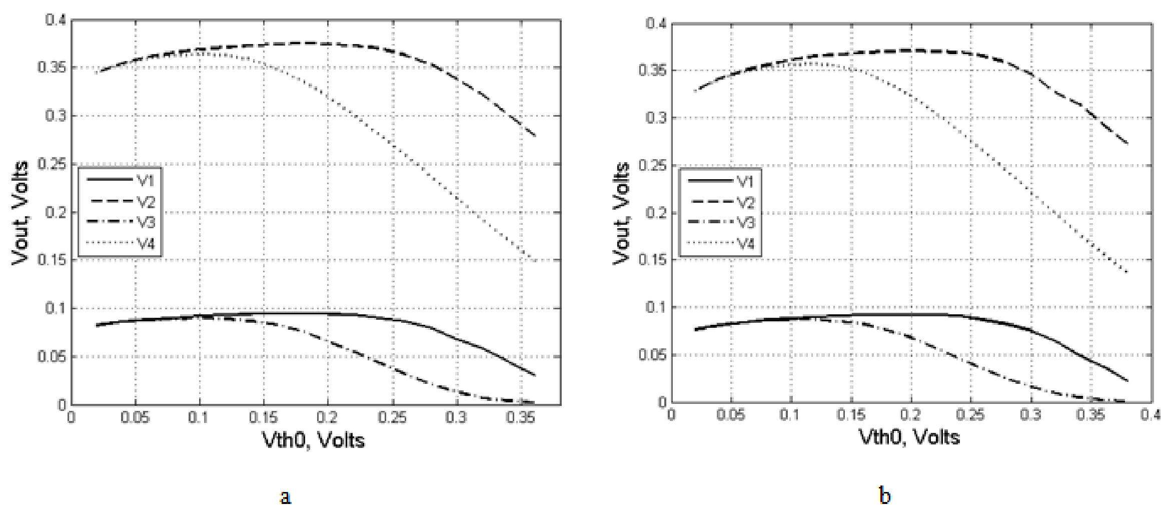


**Figure4.** S*ingle-stage multiplier output voltage versus threshold voltage of MOS transistors implemented using different technologies: a) 90 nm; b) 65 n, for various load resistances and input voltage amplitudes: V1) $V_{in}$ = 0.1 V, R = 1 GΩ; V2) $V_{in}$ = 0.3 V, R = 1 GΩ; V3) $V_{in}$ = 0.1 V, R = 10 MΩ; V4) $V_{in}$ = 0.3 V, R = 10 MΩ*

It is seen from Figure 4 that at certain values of VTH0 there are maximums of the output voltages. For 90 nm technology standard value of threshold voltage is VTH0 = 0.28 V, for 65 nm technology -

VTH0 = 0.2 V. For load resistance R = 1 GΩ, the optimum is VTH0 = 0.18 V for 90 nm technology and VTH0 = 0.2 V for 65 nm. At load current rising (load resistance lowering) optimum value VTH0 is shifted to the domain of lower values. At R = 10 MΩ, for 90 nm the optimum is VTH0 = 0.1 V and for 65 nm VTH0 = 0.12 V. Additionally one can notice significant decreasing of the output voltage with growth of VTH0 with respect to the optimum value while reduction of VTH0 leads to more smooth voltage variation, which is proved by the analysis of equations (1) – (3).

The MOS transistor sizes (relation of channel width W to its length L) impact on the output voltage level of the single-stage multiplier was investigated. The simulation results obtained with Tanner EDA for different technologies, various load resistances and input voltages amplitudes are shown on Figure 5.

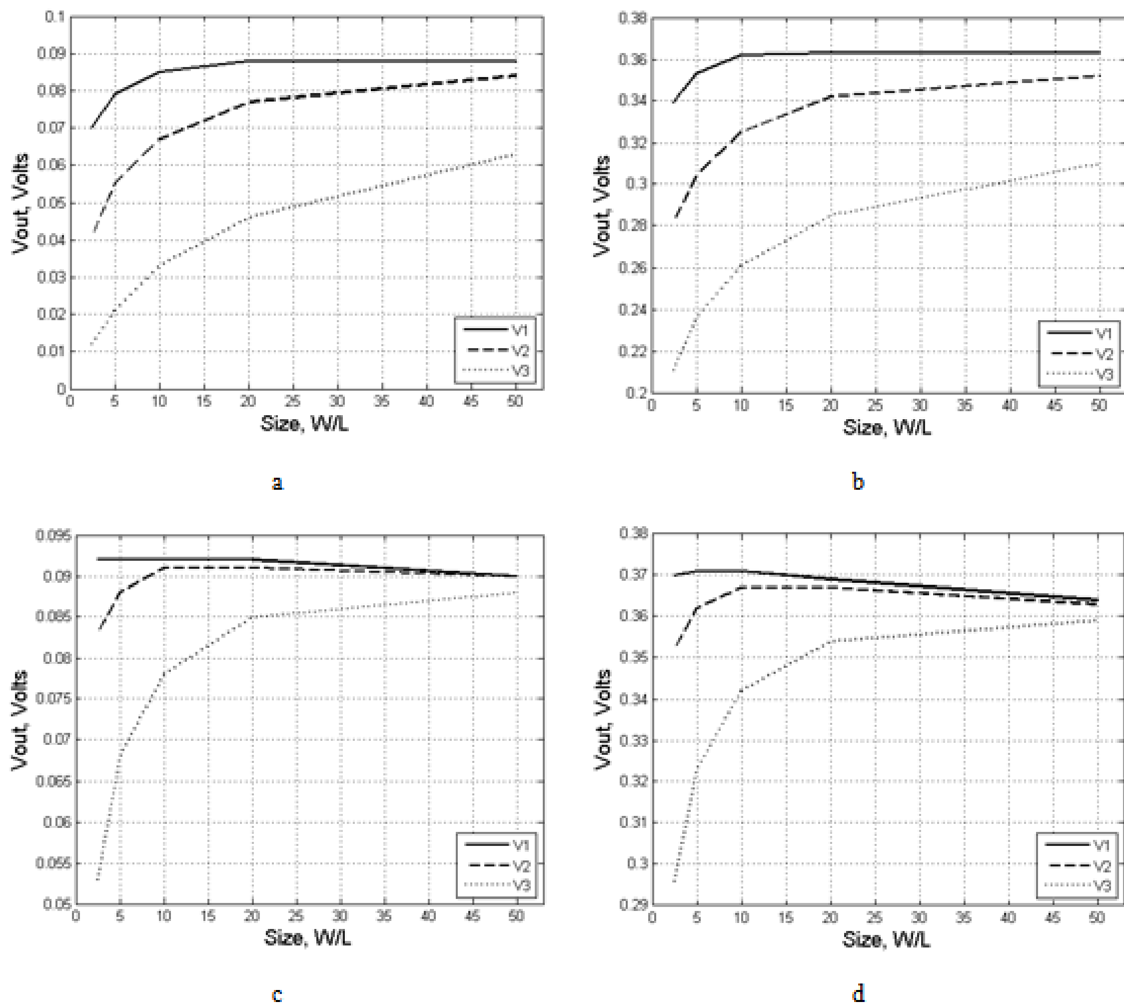


**Figure5.** *Single-stage multiplier output voltage versus sizes of MOS transistors implemented using different technologies for various input voltages: a) 90 nm, $V_{in}$ = 0.1 V; b) 90 nm, $V_{in}$ = 0.3 V; c) 65 nm, $V_{in}$ = 0.1 V; d) 65 nm, $V_{in}$ = 0.3 V, and for various load resistances: V1), R = 1 GΩ; V2) R = 100 MΩ; V3) R = 10 MΩ*

It is seen from Figure 5 that for 90 nm technology the increasing of W/L relation leads to rising of the output voltage level since with growth of W the forward currents of diodes, which charge the capacitors, are also increasing. Deceleration and the following ending of the output voltage growth can be explained by the fact that at the cost of enlarging transistors p-n junctions' area at certain value W/L the diode reverse currents, which discharge the capacitors, become comparable in order of magnitude with forward currents. With increasing of W/L the capacitances of transistors' p-n junctions also increase as well as related with them capacitive losses. For 65 nm technology and high load resistances the reverse currents and p-n junctions' capacitances have considerable impact already at rather small W/L resulting in the output voltage level decreases with increasing of transistor sizes.

Results obtained (see Figures 2, 4, 5) show the possibility of multipliers operation in transistor subthreshold region when in the charge storage cycle the storage capacitor is charging by small

currents during long time and then in the operating cycle the stored charge is used for microcircuit power supplying [22-24]. Such protocol allows to ensure the possibility of operation at low input voltages and meets requirement of functioning the passive wireless microdevices at considerable distances from the base station or in the case of harvesting energy from the environment [24].

## 4. Conclusion

The research of different configurations of energy converters which find application in the passive wireless devices has been conducted in this paper. It was determined that among the reviewed configurations of base cells based on nanoscale MOS transistors the highest performance is provided be single-stage voltage multiplier. The increasing of the output voltage can be attained by adding the multiplier stages. For this configuration the impact of threshold voltage and sizes of transistor on the output voltage with respect to various load resistances, input voltage amplitudes and using technology was investigated. The results of the work could be useful for developers of passive wireless microdevices, e.g. RFID tags.

The work is performed with financial support from ‘Southern Federal University Development Program till 2021 year’ (VnGr-07/2017-10 project).

## References

[1] Tran L.-G., Cha H.-K., Park W.-T. RF power harvesting: a review on designing methodologies and applications, Micro and Nano Systems Letters, 2017, Vol. 5, No. 14, pp. 1-16.

[2] Takacs A., Okba A., Aubert H., Charlot S., Calmon P-F. Recent advances in electromagnetic energy harvesting and Wireless Power Transfer for IoT and SHM applications, 2017 IEEE International Workshop of Electronics, Control, Measurement, Signals and their Application to Mechatronics. IEEE, 2017, pp. 1-4.

[3] Gudan K., Shao S., Hull J.J., Ensworth J., Reynolds M.S. Ultra-low Power 2.4GHz RF Energy Harvesting and Storage System with -25dBm Sensitivity, 2015 IEEE International Conference on RFID (RFID), 2015, pp. 40-46.

[4] Almohaimeed A.M., Amaya R.E., Lima J.A., Yagoub M.C.E. An Adaptive Power Harvester with Active Load Modulation for Highly Efficient Short/Long Range RF WPT Applications, Electronics, 2018, Vol. 7, No. 125, pp. 1-14.

[5] Gutierrez F. Fully-Integrated Converter for Low-Cost and Low-Size Power Supply in Internet-of-Things Applications, Electronics, 2017, Vol. 6, No. 38, pp. 1-20.

[6] Valenta C.R. Microwave-Energy Harvesting at 5.8 GHz for Passive Devices: Ph. D. Thesis. USA, GA, Atlanta, 2014, 215 p.

[7] Liu D., Wang R., Yao K. Design and Implementation of a RF Powering Circuit for RFID Tags or Other Batteryless Embedded Devices, Sensors (Basel), 2014, Vol. 14, No. 8, pp. 14839-14857.

[8] Liu H., Bolic M., Nayak A., Stojmenovic I. Taxonomy and Challenges of the Integration of RFID and Wireless Sensor Networks, IEEE Network, 2008, Vol. 22, No. 6, pp. 26-35.

[9] Zhao P. Energy Harvesting Techniques for Autonomous WSNs/RFID with a Focus on RF Energy Harvesting: Doctor’s degree Dissertation. Germany, Darmstadt, 2012, 138 p.

[10] Olgun U., Chen C.-C., Volakis J.L. Wireless Power Harvesting with Planar Rectennas for 2.45 GHz RFIDs, 2010 URSI International Symposium on Electromagnetic Theory. IEEE, 2010, pp. 329-331.

[11] Hua X., Harjani R. A 5μW-5mW Input Power Range, 0-3.5V Output Voltage Range RF Energy Harvester with Power-Estimator-Enhanced MPPT Controller, 2018 IEEE Custom Integrated Circuits Conference (CICC), 2018, pp. 1-4.

[12] Sheu M.-L., Tiao Y.-S., Fan H.-Y., Huang J.-J. Implementation of a 2.45GHz Passive RFID Transponder Chip in 0.18μm CMOS, Journal of Information Science and Engineering, 2010, Vol. 26, pp. 597-610.

[13] Fahsyar P.N.A., Soin N. A Proposed Low Power Voltage Multiplier for Passive UHF RFID Transponder, 2010 IEEE International Conference on Semiconductor Electronics, 2010, pp. 334-337.

[14] Mazzilli F., Thoppay P.E., Jöhl N., Dehollain C. Design Methodology and Comparison of Rectifiers for UHF-band RFIDs, IEEE Radio Frequency Integrated Circuits Symposium, 2010, pp. 505-508.

[15] Valenta C.R., Durgin G.D. Harvesting Wireless Power: Survey of Energy-Harvester Conversion Efficiency in Far-Field, Wireless Power Transfer, IEEE Microwave Magazine, 2014, Vol. 15, No. 4, pp. 108–120.

[16] Patil P.R., Bedekar P.P. Analysis & Design of Active RFID Tag, Network and Complex Systems, 2014, Vol. 4, No. 4, pp. 47-51.

[17] Dobkin D.M. The RF in RFID: Passive UHF RFID in Practice. USA, MA, Burlington: Elsevier, 2008, 493 p.

[18] Tanner TSpiceSimulation[Online].Available:http://s3.mentor.com/public_documents/datasheet/tannereda/tspiceds.pdf (Accessed 20November 2019).

[19] Hu C., Niknejad A.M., Paydavosi N. BSIM4v4.8.0 MOSFET Model – User's Manual. USA, CA, Berkeley: University of California, 2013, 177 p.

[20] Sicard E., Bendhia S.D. Basics of CMOS Cell Design. USA: McGraw-Hill, 2007, 429 p.

[21] Reynders N., Dehaene W. Ultra-Low-Voltage Design of Energy-Efficient Digital Circuits. Switzerland: Springer, 2015, 192 p.

[22] Wang A., Calhoun B.H., Chandrakasan A.P. Sub-threshold Design for Ultra Low-Power Systems. USA, NY, New York: Springer, 2006, 209 p.

[23] Vaddi R., Dasgupta S., Agarwal R.P. Device and Circuit Design Challenges in the Digital Subthreshold Region for Ultralow-Power Applications, VLSI Design, 2009, Article ID 283702, pp. 1-14.

[24] Konoplev B.G., Sinyukin A.S. Research of Rectifiers Based on Nanoscale MOS Devices for Microsystems with Wireless Power Supply, Izvestiya SFedU. Engineering Sciences, 2018, No. 2 (196), pp. 105-113.

**Citation:** *Boris G. Konoplev, Alexander S. Sinyukin, "Research of Nanoscale MOSFET Parameters Impact on the Performance of Energy Converters for Internet of Things." International Journal of Innovative Research in Electronics and Communications (IJIREC), 6(4), pp.18-24. http://dx .doi.org /10.20431/2349-4050.0604002*

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